72. The method of claim 71 wherein:

(e) said constructing step (d) comprises: providing a selected pattern of interconnection by filling a corresponding pattern of solder dot connections.

73. The method of claim 71 wherein:

(f) said constructing step (d) comprises: providing a selected pattern of interconnection by installing a corresponding pattern of jumper wires.

74. The method of claim 71 further comprising:

(g) testing said so constructed module as to its operational status to approve use of said module or to identify any operating problem in said module; and

(h) reconstructing said module to remove any identified operating problem;

(i) testing said module as to its operational status to approve use as reconstructed or to identify any operating problems; and

(d) repeating steps (h) and (i) as required until the module is approved for service.

75. A memory module constructed in accordance with any of the claims ~~71 through 74~~.

---

*Discussion*

**Information Disclosure Statement by Applicant**

The Information Disclosure Statement submitted herewith covers four U.S. patents cited in the copy of PCT application PCT/US97/14204 which was published on February 19, 1998. The International Search Report classifies the cited patent as as being in category "A", i.e., "documents defining the general state of the art which are not considered to be of particular relevance." Copies of the four patents are submitted herewith. The four cited patents have been carefully studied and it is believed that they are not relevant to the allowance of any claim now in this application. The Examiner is requested to include these newly cited references in his consideration of the claims now in this application.

Specifically, Chiu relates to testing and burn in-of devices on a wafer, removal of defective devices, and replacement with good devices.

Usami , replaces defective macro cells before integration into larger collections of components. Usami replaces in total, as opposed to substitution of defective lines in one unit with operational lines from an independent unit.

Friedman studies the patterns of occurrence of defects in wafers to find possible correlation between defect mapping in a wafer and the process steps in forming the structures on the wafer.

Logue constructs "A" and "B" wafers which are mirror images. Defective circuits on "A" wafers are physically replaced with operational circuits removed from a "B" wafer.

**The Claims as Amended and the newly added claims**

Applicant respectfully submits that the amendments to the claims presented herein overcome: (a) the Examiner's objections to claims 1 and 33; (b) the basis of rejection of claims 24, 31, and 65 under 35 U.S.C. 112; and (c) the basis of rejection of claims 1 - 18, 50, - 52, and 65 under 35 U.S.C. 102(b) as anticipated by Daughton. Each of the independent rejected claims, namely 1, 8, 12, and 50 , as now amended distinguishes applicant's invention over Daughton and over any prior art known to the applicant. Similarly, the newly added claims 66 through 75 distinguish applicant's claimed invention over Daughton and any prior art known to the applicant.

Applicant respectfully requests entry of the amendments presented herein; reversal of the various objections and rejections presented in the present office action; and allowance of claims 1 - 75 as now presented. Should the Examiner be of the view that a telephone or personal interview would be helpful in advancing prosecution of this application, the undersigned will welcome a call at (630) 377 2415. If I am not in my office, please leave a message on my answering machine.

Respectfully,

John C. Albrecht 10/1/99

John C. Albrecht (Reg. 18,373)